



Express Mail Receipt No. ED638708299US  
deposited on June 30, 2005

PATENT  
Dkt. STL11422

**IN THE UNITED STATES PATENT AND TRADEMARK OFFICE**

In re application of: **Robert G. Bean, Clark E. Lubbers and Randy L. Roberson**  
Assignee: **SEAGATE TECHNOLOGY LLC**  
Application No.: **10/669,196** Group No.: **2184**  
Filed: **September 23, 2003** Examiner:  
For: **DATA RELIABILITY BIT STORAGE QUALIFIER AND LOGICAL UNIT METADATA**

**Mail Stop Petition**  
**Commissioner for Patents**  
**P.O. Box 1450**  
**Alexandria, VA 22313-1450**

**PETITION TO MAKE SPECIAL FOR NEW APPLICATION  
UNDER M.P.E.P. § 708.02, VIII**

**1. Petition**

Applicant hereby petitions to make this new application, which has not received any examination by the Examiner, special.

**2. Claims**

All the claims in this case are directed to a single invention. If the Office determines that all the claims presented are not obviously directed to a single invention, then applicant will make an election without traverse as a prerequisite to the grant of special status.

**3. Search**

A search has been made by professional searcher in the following:

Field of search: Errors  
Class/Subclasses  
714/005, 006, 013, 758 and 763

A copy of the search report from Mark Spector, professional searcher, is submitted herewith.

**4. Copy of references**

All of the references most closely related to the subject matter encompassed by the claims are of record or are listed in the Supplemental Information Disclosure Statement which accompanies this Petition, in accordance with M.P.E.P. 708.02VIII(D).

Also included with the Supplemental Information Disclosure Statement is Form PTO/SB/08A (Substitute for PTO-1449) and copies of the references listed therein.

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**5. Detailed discussion of the references**

There is submitted herewith a detailed discussion of the references, which discussion particularly points out how the claimed subject matter is distinguishable over the references.

Also attached is an Information Disclosure Statement.

**6. Fee**

The fee required by 37 C.F.R. 1.17(h) \$130.00 is to be paid by:

Authorization is hereby made to charge the amount of \$130.00 to Credit card as shown on the attached credit card information authorization form PTO-2038.

Charge any additional fees required by this paper or credit any overpayment to Deposit Account No. 06-0540. A duplicate of this paper is attached.

Date: 6/30/2005

Respectfully submitted

A handwritten signature consisting of two stylized initials, possibly "M" and "K", followed by a surname.

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**DETAILED DISCUSSION OF THE REFERENCES IN SUPPORT OF  
PETITION TO MAKE SPECIAL FOR NEW APPLICATION  
UNDER M.P.E.P. § 708.02, VIII**

Sir:

The embodiments of the present invention as claimed by the independent claims are characterized, at least without limitation, by the following recited features:

Claim 1

*A method for storing data comprising the step of storing first information with first data, wherein the first information directly indicates the status of the first data.*

(claim 1)

None of the references of record teach or suggest the claimed apparatus whereby the first information directly indicates the status of the first data.

U.S. Pats. 5,379,411 and 5,574,856 to Morgan disclose providing indicator bits to log retrospectively when and what data was affected by an error. Morgan contrarily discloses a passive logging solution, not related to identifying the status of data before processing it, and thereby avoiding the processing error.

U.S. Pat. 5,504,858 to Ellis is also a passive logging solution that discloses using parity metadata that does not directly indicate the status of the associated data. This is clearly seen in the sequence of FIG. 6 wherein the failure in block 64 precedes the use of the metadata in block 78.

U.S. Patent 6,282,686 discloses associating a bit with a component and grouping components logically. Again, the bit indicates the occurrence of an error, but does not directly indicate the status of the component until after an error has occurred.

Claim 8

*A method for protecting data comprising the step of accompanying first information with first data, wherein the first information indicates status of second data associated with the first data.*

(claim 8)

Claim 15

*circuitry configured to perform at least one of a group consisting of a reading and a writing of the storage areas, wherein at least one of the storage areas includes first information accompanying first data, wherein the first information indicates status of second data associated with the first data.*

(excerpt of claim 15)

None of the references of record teach or suggest the claimed apparatus whereby information first information indicates the status of second data associated with the first data. All the references disclose using the logging indicators to indicate an error has occurred in relation to the data that the logging indicator was associated with.

None of the references of record disclose or suggest the novelty of the embodiments of the present invention as recited by the language of the independent claims. Furthermore, there is no motivation from the references to modify and/or combine one or more references to arrive at the embodiments of the present invention as claimed. Accordingly, the references of record cannot sustain a Section 102 or 103 rejection.

It is submitted that all of the elements set forth in M.P.E.P. §708.02 subsection VIII have now been provided in this petition to make special. It is requested that this petition be granted and that the presented claims be examined as soon as possible.

Respectfully submitted,

Date: 6/30/2005

By:



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RE: Data Reliability Bit Storage Qualifier & Logical Unit Metadata STL11422

Dear Mr. McCarthy:

6.12.05

In response to your letter of 5.03, a patent search has been conducted regarding the three independent claims of STL11422, and in particular for a method for storing embedded or appended reliability qualifier information bits indicating the status and reliability of stored data, in a RAID configuration.

A search in US Patents was conducted in:

Errors, Class 714, Subclasses: 005, 006, 013, 758 and 763.

US Patent Examiner G. Lamarre au2133, was consulted.

The following 15 US Patents and Pub disclose embedded appended indicators, as noted.

6829308 Eroz : "Clm1. A method for *reliably* communicating over a satellite in support of a communication service, the method comprising: encoding an input message to output a structured *Low Density Parity Check coded message* that provides storage of adjacent relevant edge values together in memory for concurrent memory access, wherein the adjacent relevant edge values are associated with a group of bit nodes or a group of *check nodes*..."

6615387 Williamson/ Seagate : "Clm1. A method for *error correction*...(a) receiving a data signal wherein the data signal includes *user data appended with a first set of parity symbols* to form a *first codeword that is appended* with a second set of parity symbols to form at least a second codeword, such that a symbol size of the first set of parity symbols is greater than a symbol size of the second set of parity symbols; (b) calculating syndrome signals from the first codeword; (c) *receiving an error signal* for each correction of the data signal..."

6523114 Barton : "The invention relates to digital data, including digital audio, video, and image data. More particularly, the invention relates to a method and apparatus for *embedding authentication data within such digital data* in a way that avoids detection by a casual observer and that allows a user to determine whether the digital data have been modified from their intended form."

6446079 Tooker : "Clm5. A protocol as defined in claim 4 wherein said *qualifier bitmap is appended* to a command issued by said network management system, and one or more bits of the bitmap may be set by giving it a designated value of 1 (one) or 0 (zero)."

6282686 Cypher : "The bits of a data block are assigned to a plurality of logical groups such that at most one bit corresponding to a component is assigned to a logical group. This assignment ensures that a component failure may introduce at most one bit error to a logical group. Each logical group uses a single error correcting code to detect and correct bit errors. *A parity bit is appended to a data block that includes a plurality of logical groups.* The parity bit may be used in conjunction with the single error correcting codes to determine whether a detected error is a single bit error or a multiple bit error."

6161192 Lubbers : "Clm1. A method for formatting a *RAID array* of storage devices with device *metadata...FE bit indicating* whether or not a corresponding *RAIDed block is consistent and thereby indicating useability...*" Lubbers also has US5774643 (RAID metadata).

5574856 Morgan : "These procedures typically include the use of *various check bytes that are appended to the data at all levels of the data transfer operation.* Specifically, in transferring data from the host system to the storage array, check bytes may be generated by the host and appended to each block of data received. Such check bytes are checked by the array storage system to determine the accuracy of the data block. Additionally, check bytes are appended to the data bytes during transfer between components of the storage array, such as to device controllers that are involved in reading/writing of data on the storage devices."

5511078 Barucchi : "Clm1. A method for correcting errors in a memory organized in words comprising N B-bit blocks ...*appending the computed error correction bits to the data bits* to form a write word storing the write word at the addressed location of the memory, for each word read from memory, testing the word for an error using the error correction bits stored with the word, correcting an error if found in a read word..."

5504858 Ellis : "If the *parity metadata bit* is in the set state, this indicates that the corresponding parity block may not be consistent with the data blocks that it describes and therefore cannot be used to regenerate data. If the parity metadata bit is in the clear state, then the corresponding parity block is consistent with the data blocks that it describes and can be used to *regenerate data.*"

5379411 Morgan : "In one embodiment, data blocks are generated by the array storage system from data received from the host system and the *code byte is appended to each block of data*, together with check bytes. When a fault occurs, predetermined code bits of the code byte are set or reset, depending upon the particular operation in progress."

Mark Spector  
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06.12.05

4837675 Robert Bean : "A secondary storage facility having a drive and a controller employing *multiple error recovery techniques*..."

4811279 Robert Bean : "1. A secondary storage system for a data processing system ...a continuous transmission of sequences of bit-multiplexed, bit-serial, real-time, signals, each of said sequences being *indicative of a set of status variables* that define the state of the controller..."

4345328 White : "Apparatus for and method of providing single bit error correction and double bit error detection using through checking parity bits. A coding scheme is implemented which uses through *checking parity bits appended to each byte as check bits*."

20050066230 Bean : "data reliability bit storage"

20040064779 Vasic/ Seagate : "Clm1 ...code bit reliabilities..." Vasic also has WO02099976 ("low density parity (bit) check codes for data storage").

During the course of this search, I uncovered this foreign reference.

WO0213436A1: METHOD AND SYSTEM FOR STEGANOGRAPHICALLY EMBEDDING INFORMATION BITS IN SOURCE SIGNALS 25 pages

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Assignee: AVWAY.COM INC., 12 Broad Street, Red Bank, NJ 07701, USA

Published / Filed: 2002-02-14 / 2001-08-02 App# WO2001US0024468

IPC Code: H04K 1/02;

ECLA Code: G06T1/00W; H04N1/32C19; H04N7/26E10;

Priority Number: 2000-08-09 US2000000634506

Abstract: A method and system for *embedding (E) information bits in a source signal (A)* like images, audio or video. The embedding being performed optimally for a given worst-case scenario of unintentional or intentional attack of the host signal (to remove the embedded bits), and a given distortion of the host signal due to information embedding.

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